501.32049RV1/329201392US4

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Yujiro KAJIHARA *et al.*
Serial No.	:	09/987,978
Filed	:	16 November 2001
For	:	LEAD FRAME SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE, USING THE SAME, AND METHOD OF AND PROCESS FOR FABRICATING THE TWO
Art Unit	:	2815
Examiner	:	J.B. Clark
Conf. No.	:	7905

RESPONSE TO OFFICE ACTION

Mail Stop Reissue
Commissioner for Patents
POB 1450
Alexandria, Virginia 22313-1450

1 November 2004

Sir:

In response to the *ex parte Quayle* Office Action was mailed 9 September 2004 in connection with the above-identified application, Applicant submits the following response, remarks and attachments.

PENDING/ALLOWED CLAIMS

Claims 15-27 were pending, under consideration and subject to examination in the Office Action, and are allowed in this application, as indicated at Item 5 in the Office Action Summary Form PTOL-326 and at Item 1 at page 2 of the Action. Applicant and the undersigned respectfully thank the Examiner for such indication of allowance.